What Is Claimed Is:

1. A system having at least one computer device for applications critical with regard to safety, comprising:

at least one processor unit;

a memory unit for storing process data;

a memory management unit for controlling memory accesses in the computer device;

an error detection unit for detecting errors in the memory unit;

at least one self-test unit assigned to the processor unit; and

connection means for connecting the at least processor unit to at least one of another processor unit and the memory management unit, the at least one processor unit being positioned together with the memory unit on a shared chip surface area.

2. The system as recited in claim 1, wherein the error detection unit is implemented as an error correction unit for correcting errors in the memory unit.

3. The system as recited in claim 1, wherein each processor unit is assigned a self-test unit for performing a self-test.

4. The system as recited in claim 1, wherein two processor units are coupled by the connection means, each processor unit being assigned a self-test unit.

5. The system as recited in claim 1, wherein a plurality of computer devices are connected to one another with the aid of at least one connection unit, the plurality of the computer devices having one of an equal and different number of processor units.

6. The system as recited in claim 1, wherein each memory unit is assigned one error correction unit in the computer device.

7. The system as recited in claim 1, wherein the memory management unit for controlling the memory access in the computer device and the at least one processor unit are implemented integrally as a single unit.

8. A method for process-data processing in at least one computer device having at least one processor unit for applications critical with regard to safety, comprising:

testing the at least one processor unit using at least one self-test unit assigned to the processor unit;

positioning the at least one processor unit together with a memory unit on a shared chip surface area;

connecting the at least one processor unit to at least one of another processor unit and a memory management unit using connection means in the at least one computer device;

controlling memory accesses in the at least one computer device using the memory management unit;

storing process data in the memory unit; and

detecting errors in the memory unit using an error detection unit.

9. The method as recited in claim 8, wherein errors in the memory unit are corrected using an error correction unit.

10. The method as recited in claim 8, wherein two processor units, coupled by the connection means, are each tested by assigned self-test units in the at least one computer device.

11. The method as recited in claim 8, wherein at least two computer devices having one of an equal and different number of processor units are combined using at least one connection unit.

12. The method as recited in claim 8, wherein the memory unit in the at least one computer device is checked for errors and corrected using an assigned error correction unit.

13. The method as recited in claim 8, wherein the at least one processor unit is tested using an assigned self-test unit.

14. The method as recited in claim 8, wherein the self-test unit outputs an error message via self-test unit output means to at least one of an external display unit and an error processing unit if a fault is recognized in the at least one processor unit by the assigned self-test unit.

15. The method as recited in claim 8, wherein at least two processor units exchange at least one of starting values, intermediate results, intermediate values, and final results via the connection means, and wherein the at least two processor units check the at least one of starting values, intermediate results, intermediate values, and final results for uniformity.

16. The method as recited in claim 15, wherein one of the at least two processor units outputs an error message via processor unit output means to at least one of an external display unit and an error processing unit if the processor unit detects a deviation between the final results and one of the intermediate results and intermediate values.

17. The method as recited in claim 8, wherein, if errors occur in the memory unit, an error message is output via error detection unit output means to at least one of an external display unit and an error processing unit.

18. The method as recited in claim 8, wherein, if errors occur in the memory unit, an error message is transmitted via the memory management unit to the at least one processor unit, and from the at least one processor unit the error message is

subsequently output via the processor unit output means to at least one of an external display unit and an error processing unit.